

μP Supervisor with Watchdog Timer, Power-Fail Comparator, Manual Reset and Adjustable Power-On Reset

Designed with high reset threshold accuracy and low power consumption, the ISL88705, ISL88706, ISL88707, ISL88708, ISL88716 and ISL88813 devices are microprocessor supervisors that are designed to monitor power-supply and battery functions in microprocessor systems. They can help to lower system cost, reduce board space requirements and increase the reliability of systems.

These devices provide essential functions such as supply voltage supervision by asserting a reset output during power-up and power-down as well as during brownout conditions. An auxiliary voltage monitor is provided for detecting power failures warning the system of low battery conditions or presence detection. In addition, an independent watchdog timer helps to monitor microprocessor activity every 1.6s (typical). An active-low manual reset is offered and reset signals remain asserted until V_{DD} returns to proper operating levels.

Users can increase the nominal 200ms power-on reset time-out delay by adding an external capacitor to the C_{POR} pin on the ISL88707 and ISL88708.

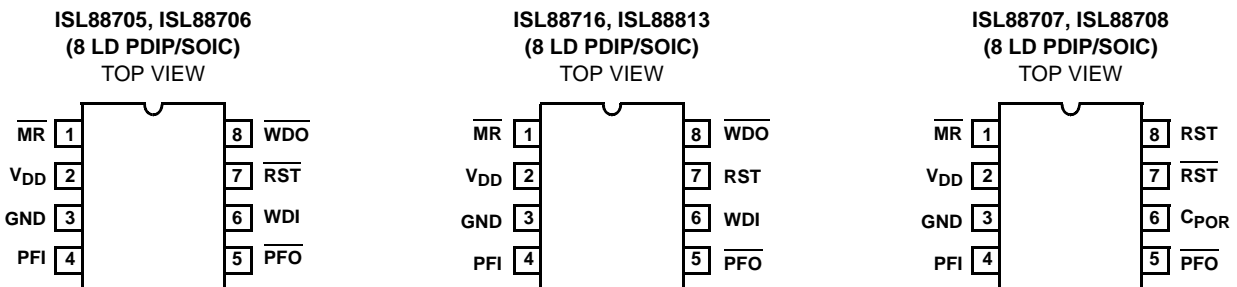
Features

- Fixed-Voltage Options Allow Precise Monitoring of +3.0V, +3.3V, and +5.0V Power Supplies
- Additional Voltage Monitor for Power-Fail Detection or Low-Battery Warning
 - Monitors Voltages Down to 1.25V
 - Adjustable Power-Fail Input Threshold
- Watchdog Timer Capability With 1.6s Time-out
- Both RST and \overline{RST} Outputs Available
- 140ms Minimum Reset Pulse Width with Option to Customize Using an External Capacitor
- Manual Reset Input on all Devices
- Reset Signal Valid Down to $V_{DD} = 1V$
- Accurate $\pm 1.8\%$ Voltage Threshold
- Immune to Power-Supply Transients
- Ultra Low 10 μ A Maximum Supply Current at 3V
- Pb-Free (RoHS Compliant)

Applications

- Portable/Battery Powered Equipment
- Notebook/Desktop Computer Systems
- Designs Using DSPs, Microcontrollers or Microprocessors
- Controllers
- Intelligent Instruments
- Communications Systems
- Industrial Equipment

Pinouts



Ordering Information

PART NUMBER (Note)	PART MARKING	V _{TH}	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL88705IP846Z	88705 I46Z	4.64V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88813IP846Z	88813 I46Z	4.64V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88707IP846Z	88707 I46Z	4.64V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88706IP844Z	88706 I44Z	4.38V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88708IP844Z	88708 I44Z	4.38V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88706IP831Z	88706 I31Z	3.09V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88708IP831Z	88708 I31Z	3.09V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88706IP829Z	88706 I29Z	2.92V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88708IP829Z	88708 I29Z	2.92V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88706IP826Z	88706 I26Z	2.63V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88716IP826Z	88716 I26Z	2.63V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88708IP826Z	88708 I26Z	2.63V	-40 to +85	8 Ld PDIP**	MDP0031
ISL88705IB846Z*	88705 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88813IB846Z*	88813 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88707IB846Z*	88707 I46Z	4.64V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB844Z*	88706 I44Z	4.38V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB844Z*	88708 I44Z	4.38V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB831Z*	88706 I31Z	3.09V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB831Z*	88708 I31Z	3.09V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB829Z*	88706 I29Z	2.92V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB829Z*	88708 I29Z	2.92V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88706IB826Z*	88706 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88716IB826Z*	88716 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15
ISL88708IB826Z*	88708 I26Z	2.63V	-40 to +85	8 Ld SOIC (Tape and Reel)	M8.15

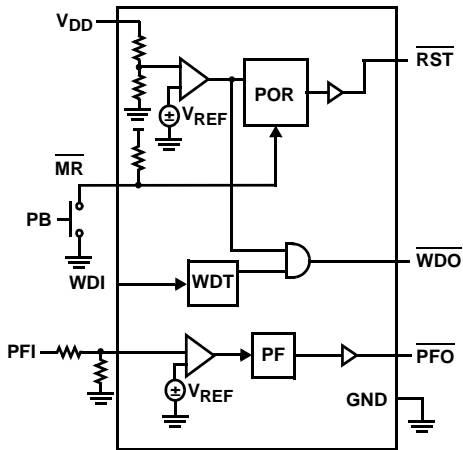
*Add "-TK" suffix for SOIC Tape and Reel Packaging. Please refer to TB347 for details on reel specifications.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

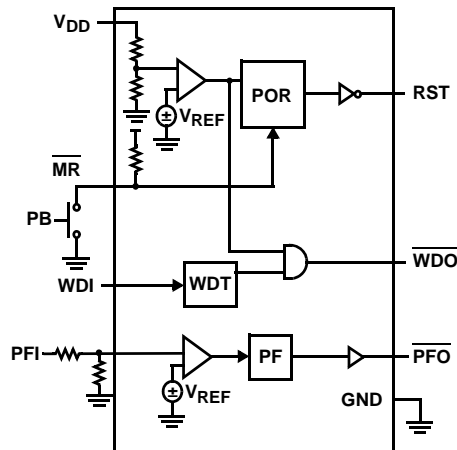
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC JSTD-020.

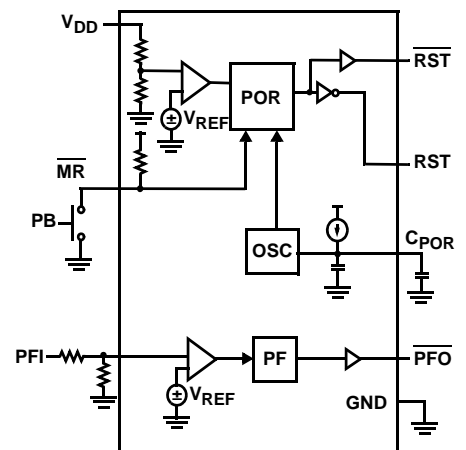
Functional Block Diagrams



ISL88705, ISL88706



ISL88716, ISL88813



ISL88707, ISL88708

Pin Descriptions

ISL88705, ISL88706	ISL88716, ISL88813	ISL88707, ISL88708	NAME	DESCRIPTION
1	1	1	$\overline{\text{MR}}$	Manual Reset Input. A reset signal is generated when this input is pulled low. The $\overline{\text{MR}}$ input is an active low debounced input to which a user can connect a push-button to add manual reset capability or drive with a signal. The MR pin has an internal 20k Ω pull-up.
2	2	2	V_{DD}	Power Supply Terminal. The voltage at this pin is compared against an internal factory-programmed voltage trip point, V_{TH1} . A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever V_{DD} falls below V_{TH1} . The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients. The voltage threshold V_{TH1} is specified in the part number suffix.
3	3	3	GND	Ground Connection
4	4	4	PFI	Power-Fail Input This is an auxiliary monitored voltage input with a 1.25V threshold that causes $\overline{\text{PFO}}$ state to follow the PFI input state.
5	5	5	$\overline{\text{PFO}}$	Power-Fail Output. This output goes high if the voltage on PFI is greater than 1.25V, otherwise $\overline{\text{PFO}}$ stays low.
		6	C_{POR}	Adjustable POR Time-out Delay Input. Connecting an external capacitor from C_{POR} to ground allows the user to increase the Power-On Reset timeout (t_{POR}) from the nominal 200ms.
6	6		WDI	Watchdog Input. The Watchdog Input takes an input from a microprocessor and ensures that it periodically toggles the WDI pin, otherwise the internal nominal 1.6s watchdog timer runs out, then reset is asserted and WDO is pulled low. The internal Watchdog Timer is cleared whenever the WDI sees a rising or falling edge or the device is manually reset. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature.
7	7	7	$\overline{\text{RST}}$	Active-Low Reset Output. The $\overline{\text{RST}}$ output is an active low output with an internal PMOS pull-up that is pulled low to GND when reset is asserted. Reset is asserted whenever: <ol style="list-style-type: none"> 1. The device is first powered up 2. V_{DD} falls below its minimum voltage sense level or 3. $\overline{\text{MR}}$ is asserted. The reset output continues to be asserted for typically 200ms after V_{DD} rises above the reset threshold or $\overline{\text{MR}}$ input goes from low to high. A watchdog time-out will not trigger a reset unless WDO is connected to $\overline{\text{MR}}$.
		8	RST	Active-High Reset Output. The RST pin functions identically to its complementary $\overline{\text{RST}}$ output but is an active high push-pull output. RST is set high to V_{DD} when reset is asserted. See the RST in "Pin Descriptions" on page 4 for more details on conditions that cause a reset.
8	8		$\overline{\text{WDO}}$	Watchdog Output. This output is pulled low when the nominal 1.6s internal Watchdog Timer expires and does not go high again until the watchdog is cleared. WDO also goes low during low V_{DD} conditions. Whenever V_{DD} is below the reset threshold, WDO stays low. However, unlike RESET, WDO does not have a minimum pulse width. As soon as V_{DD} rises above the reset threshold, WDO goes high with no delay.

Absolute Maximum Ratings

Temperature Under Bias-40°C to +125°C
 Storage Temperature-65°C to +150°C
 Voltage on any Pin with Respect to GND-1.0V to +7V
 DC Output Current 5mA

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 PDIP Package* (4-layer test board) 83
 SOIC Package (4-layer test board) 110
 Pb-free reflow profilesee link below
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>
 *Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Recommended Operating Conditions

Temperature Range (Industrial)-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{DD}	Supply Voltage Range		2.0		5.5	V
I _{DD}		V _{DD} = 5V, WDT Inactive		10	19	μA
		V _{DD} = 3V, WDT Inactive		8	10	μA
I _{LI}	Input Leakage Current (PFI)				100	nA
I _{LO}	Output Leakage Current				100	nA
VOLTAGE THRESHOLDS						
V _{TH1}	Fixed V _{DD} Voltage Trip Point		4.556	4.640	4.724	V
			4.301	4.380	4.459	V
			3.034	3.090	3.146	V
			2.867	2.920	2.973	V
			2.583	2.630	2.677	V
V _{TH1HYST}	Hysteresis at V _{TH1} Input Temperature = +25°C	V _{TH1} = 4.64V		46		mV
		V _{TH1} = 4.38V		44		mV
		V _{TH1} = 3.09V		37		mV
		V _{TH1} = 2.92V		29		mV
		V _{TH1} = 2.63V		31		mV
RST AND $\overline{\text{RST}}$						
V _{OL}	Reset Output Voltage Low	V _{DD} ≥ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V _{DD} < 3.3V, Sinking 1.5mA		0.05	0.40	V
V _{OH}	RST Output Voltage High	V _{DD} ≥ 3.3V, Sourcing 2.5mA	V _{DD} - 0.6	V _{DD} - 0.4		V
		V _{DD} < 3.3V, Sourcing 1.5mA	V _{DD} - 0.6	V _{DD} - 0.4		V
	$\overline{\text{RST}}$ Output Voltage High	V _{DD} ≥ 3.3V, Sourcing 0.8mA	V _{DD} - 0.6	V _{DD} - 0.4		V
		V _{DD} < 3.3V, Sourcing 0.5mA	V _{DD} - 0.6	V _{DD} - 0.4		V
t _{RPD}	V _{TH} to Reset Asserted Delay			45		μs
t _{POR}	POR Time-Out Delay	C _{POR} is open	140	200	260	ms
C _{LOAD}	Load Capacitance on Reset Pins			5		pF
MANUAL RESET						
V _{MRL}	$\overline{\text{MR}}$ Input Voltage Low				0.8	V
V _{MRH}	$\overline{\text{MR}}$ Input Voltage High		V _{DD} - 0.6			V

Electrical Specifications Over the recommended operating conditions unless otherwise specified. (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{MR}	\overline{MR} Minimum Pulse Width		550			ns
R_{PU}	Internal \overline{MR} Pull-Up Resistor			20		k Ω
WATCHDOG TIMER (Note 2)						
t_{WDT}	Watchdog Time-out Period		1.0	1.6	2.0	s
t_{WDPS}	WDI Minimum Pulse Width		100			ns
V_{IL}	Watchdog Input Voltage Low				$0.3 \times V_{DD}$	V
V_{IH}	Watchdog Input Voltage High		$0.7 \times V_{DD}$			V
V_{WDOL}	\overline{WDO} Output Voltage Low	$V_{DD} \geq 3.3V$, Sinking 2.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$, Sinking 1.5mA		0.05	0.40	V
V_{WDOH}	\overline{WDO} Output Voltage High	$V_{DD} \geq 3.3V$, Sourcing 2.5mA	$V_{DD} - 0.6$	$V_{DD} - 0.4$		V
		$V_{DD} < 3.3V$, Sourcing 1.5mA	$V_{DD} - 0.6$	$V_{DD} - 0.4$		V
I_{WDT}	Watchdog Input Current				1	μA
POWER-FAIL DETECTION						
V_{THPFI}	PFI Input Threshold Voltage		1.20	1.25	1.30	V
$PFIV_{THYST}$	Hysteresis Voltage			20		mV
V_{PFOL}	PFO Output Voltage Low	$V_{DD} \geq 3.3V$, Sinking 2.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$, Sinking 1.5mA		0.05	0.40	V
V_{PFOH}	PFO Output Voltage High	$V_{DD} \geq 3.3V$, Sourcing 2.5mA	$V_{DD} - 0.6$	$V_{DD} - 0.4$		V
		$V_{DD} < 3.3V$, Sourcing 1.5mA	$V_{DD} - 0.6$	$V_{DD} - 0.4$		V

NOTE:

2. Applies to ISL88705, ISL88706, ISL88716, and ISL88813.

Principles of Operation

The ISL88705, ISL88706, ISL88707, ISL88708, ISL88716, ISL88813 devices provide those functions needed for monitoring critical voltages such as power-supply and battery functions in microprocessor systems. Features of these supervisors include Power-On Reset control, Supply Voltage Supervision, Power-Fail Detection and Manual Reset Assertion. The integration of all these features along with high reset threshold accuracy and low power consumption make these devices ideal for portable or battery-powered equipment.

Power-On Reset (POR)

Applying power to the device activates a POR circuit which asserts reset (i.e. \overline{RST} goes high while RST goes low). These signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signals remain active until V_{DD} rises above the minimum voltage sense level for time period t_{POR} . This ensures that the supply voltage has stabilized to sufficient operating levels.

Low Voltage Monitoring

These devices monitor both the voltage level of V_{DD} and an auxiliary voltage on PFI.

When IC is initially biased reset is asserted until the V_{DD} voltage is greater than the specific IC fixed-voltage trip point for the t_{POR} duration of 200ms. At any subsequent time that V_{DD} does not exceed its voltage threshold, reset is once again asserted, i.e. \overline{RST} is high and RST is low. See Figure 1.

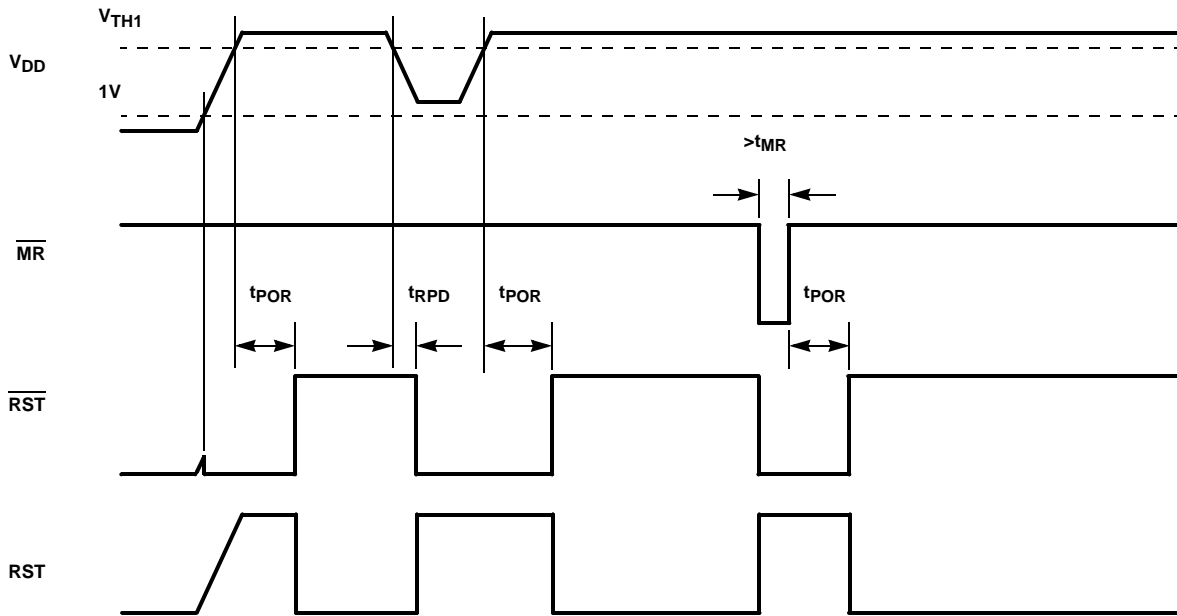


FIGURE 1. POWER-SUPPLY MONITORING TIMING DIAGRAM (WDI TRI-STATED)

Power Failure Monitor

These devices also have a Power-Failure Monitor that helps to monitor an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, detect a low-battery condition, presence detection or simply monitor a power supply other than +5V. The 1.25V threshold detector can be adjusted using an external resistor divider network to provide custom voltage monitoring of voltages greater than 1.25V, according to Equation 1 (see Figure 2):

$$PFI V_{TH} = 1.25 \left(\frac{R_1 + R_2}{R_2} \right) \quad (EQ. 1)$$

PFO goes low whenever PFI is less than the 1.25V (or user-set) threshold voltage.

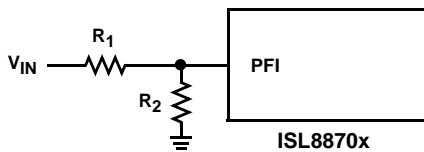


FIGURE 2. CUSTOM VTH WITH RESISTOR DIVIDER ON PFI

Adjusting tPOR

On the ISL88707 and ISL88708, users can adjust the Power-On Reset time-out delay (tPOR) to many times the nominal tPOR of 200ms. To do this, connect a capacitor between CPOR and ground (see Figure 3). For example, connecting a 50pF capacitor to CPOR will increase tPOR from 200ms to ~1.4s. Care should be taken in PCB layout and capacitor placement in order to reduce stray capacitance as much as possible, which contributes to tPOR error.

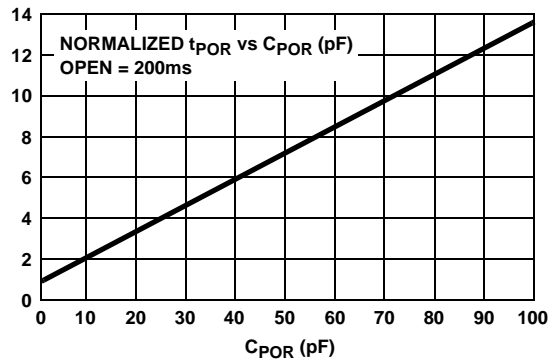
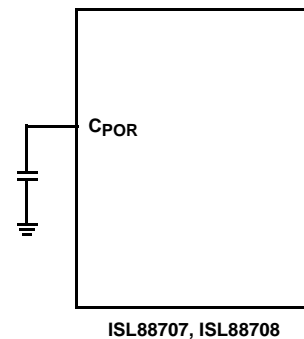


FIGURE 3. ADJUSTING tPOR WITH A CAPACITOR

Manual Reset

The manual-reset input (MR) allows the user to trigger a reset by using a push-button switch. The MR input is an active low debounced input. By connecting a push-button directly from MR to ground, the designer adds manual system reset capability (see Figure 4). Reset is asserted if the MR pin is pulled low to less than 100mV for the minimum MR pulse width or longer while the push-button is closed.

After $\overline{\text{MR}}$ is released, the reset outputs remain asserted for t_{POR} (200ms) and then released.

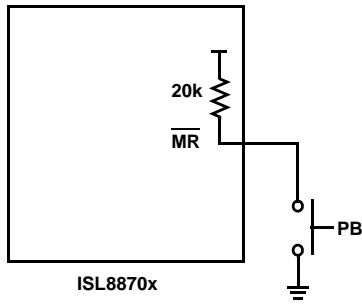


FIGURE 4. CONNECTING A MANUAL RESET PUSH-BUTTON

Watchdog Timer

The Watchdog Timer circuit checks microprocessor activity by monitoring the WDI input pin. The microprocessor must periodically toggle the WDI pin within t_{WDT} (typically 1.6s), otherwise the $\overline{\text{WDO}}$ pin goes low (see Figure 5). Internally, the 1.6s timer is cleared by either a reset or by toggling the WDI input, which can detect pulses longer than 50ns.

Whenever there is a low-voltage V_{DD} condition, $\overline{\text{WDO}}$ goes low. Unlike the reset outputs, however, $\overline{\text{WDO}}$ does not have a minimum reset pulse width (t_{POR}). $\overline{\text{WDO}}$ goes high as soon as V_{DD} rises above its voltage trip point (see Figure 5). With WDI open or connected to a tristated high impedance input, the Watchdog Timer is disabled and only pulls low when $V_{\text{DD}} < V_{\text{TH1}}$.

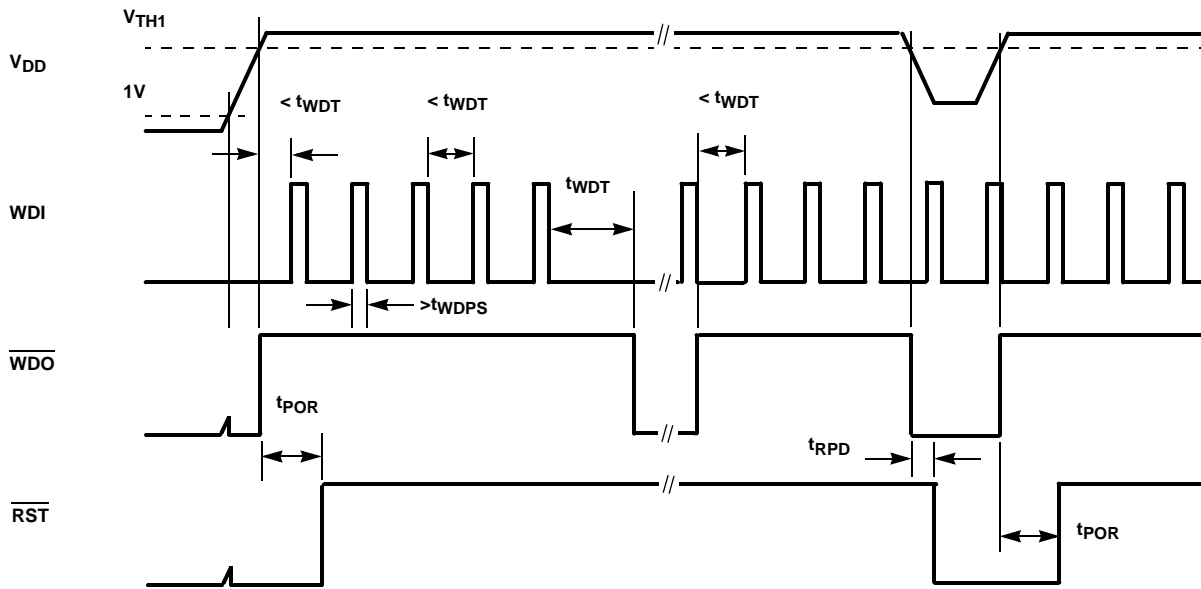


FIGURE 5. WATCHDOG TIMING DIAGRAM

Typical Performance Curves

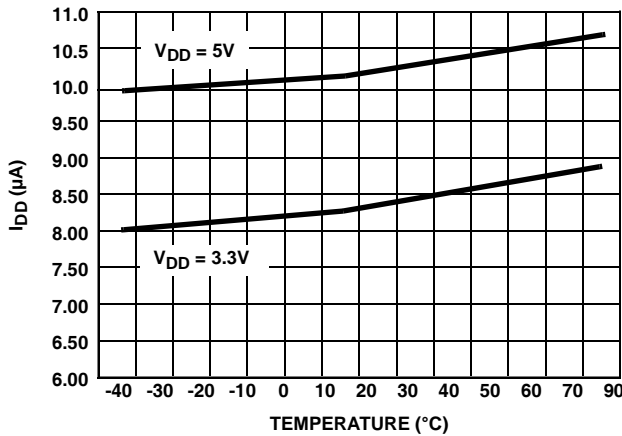


FIGURE 6. I_{DD} vs. TEMPERATURE

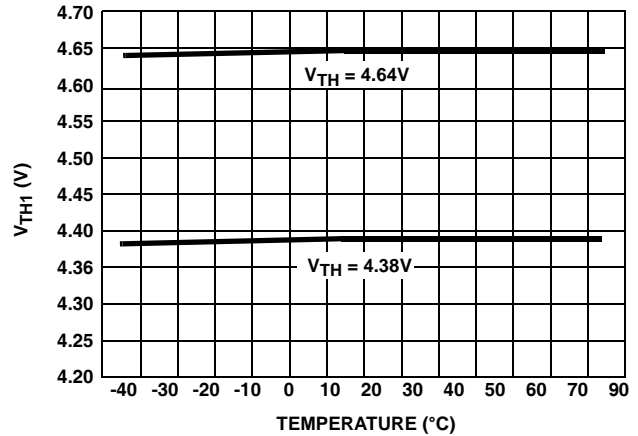


FIGURE 7. V_{TH1} vs. TEMPERATURE FOR 5V SUPPLY

Typical Performance Curves (Continued)

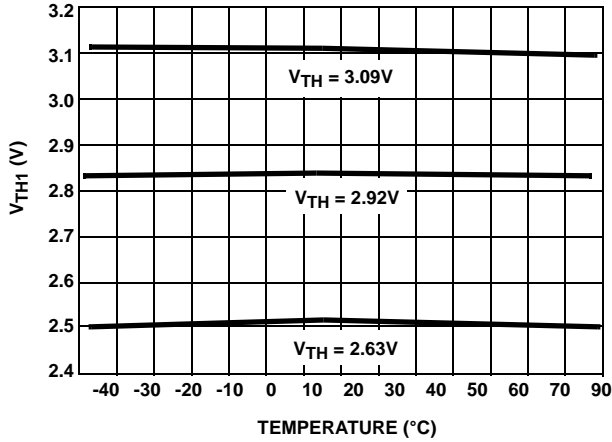


FIGURE 8. V_{TH1} vs TEMPERATURE < 5V SUPPLY

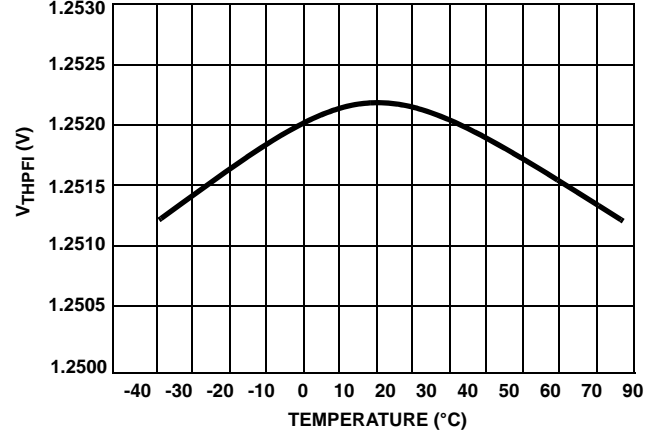


FIGURE 9. V_{THPF1} vs TEMPERATURE

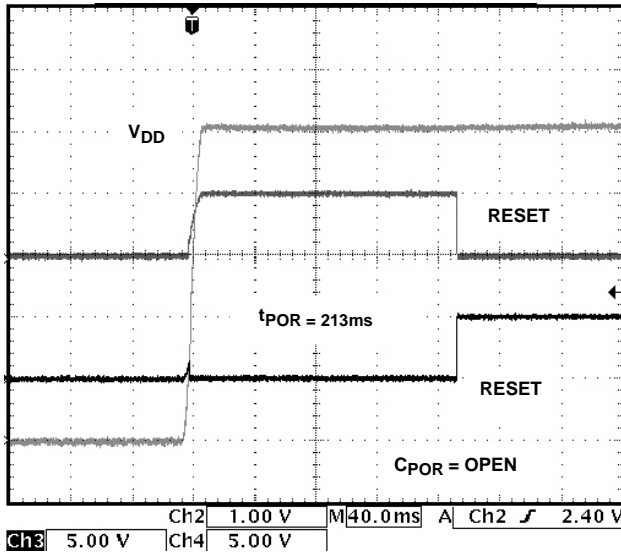


FIGURE 10. RESET AND RESET ASSERTION

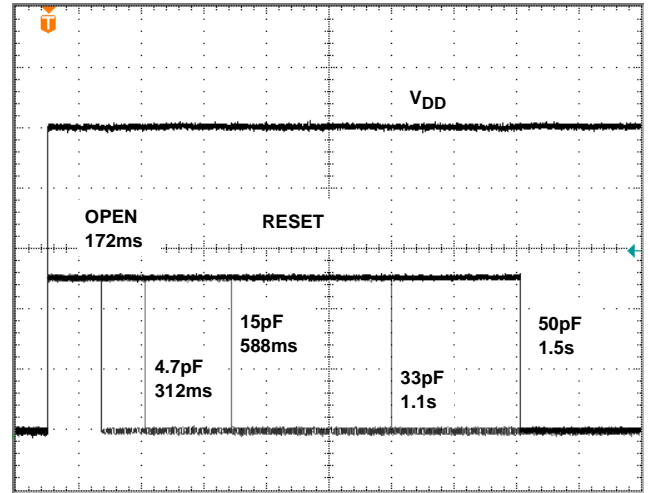


FIGURE 11. RESET ASSERTION vs C_{POR}

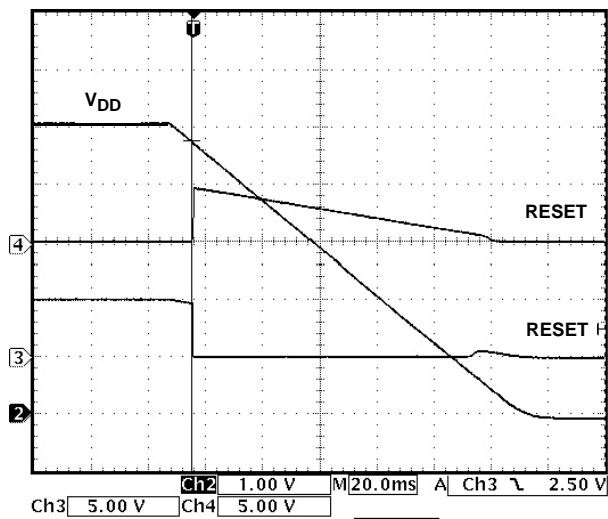


FIGURE 12. RESET AND RESET DEASSERTION

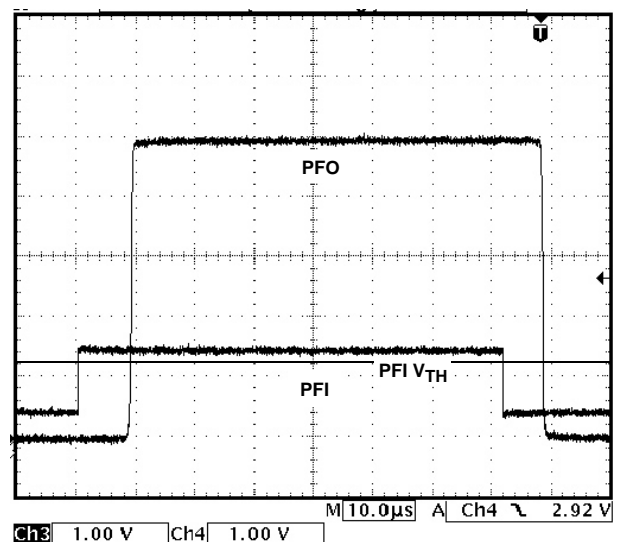


FIGURE 13. 5V PFI TO PFO RESPONSE

Bipolar Voltage Sensing

Any of the ISL88705, ISL88706, ISL88707, ISL88708, ISL88716, ISL88813 devices can be used to sense and report the presence of both a positive and negative voltage via the PFI and $\overline{\text{PFO}}$, as shown in Figure 16. The V_{DD} monitors the positive voltage as normal and the PFI monitors the presence of the negative supply. As the differential voltage across the R_1, R_2 divider is increased, the resistor values must be chosen such that the PFI node is $<1.25\text{V}$ when the $-V$ supply is satisfactory and the positive supply is at its maximum specified value. This allows the positive supply to fluctuate within its acceptable range without signaling a reset. Driving the $\overline{\text{MR}}$ with the inverted $\overline{\text{PFO}}$ signal as shown provides for reset generation when $-V$ is not satisfactorily present. Reset will remain asserted as long as $\overline{\text{PFO}}$ is high.

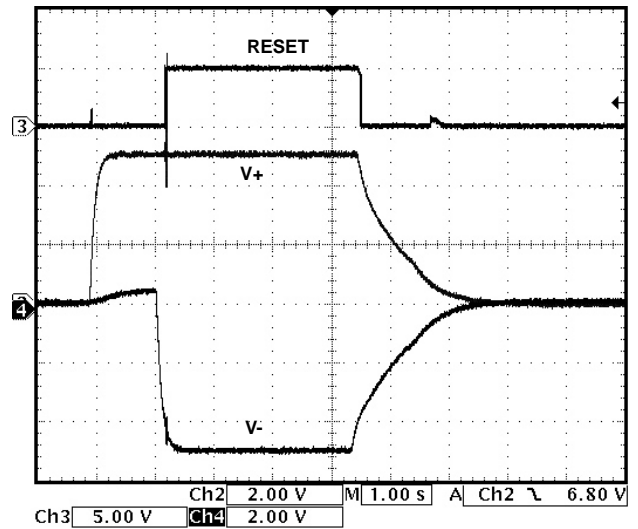
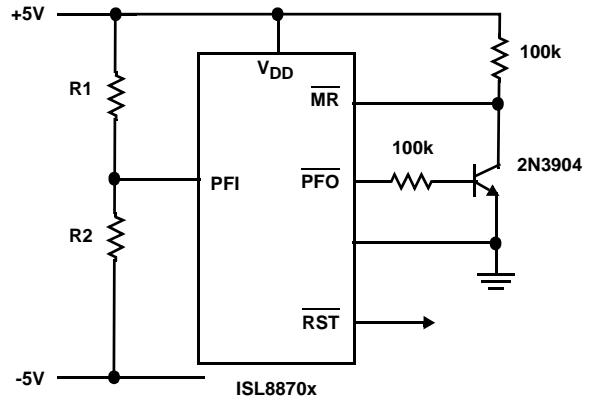
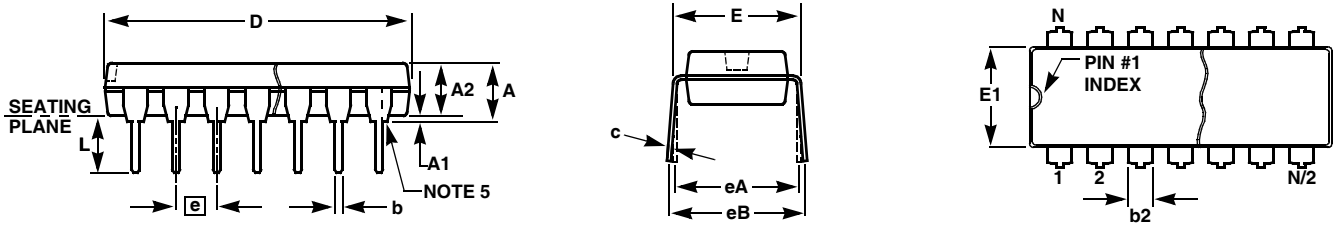


FIGURE 16. $\pm 5\text{V}$ MONITORING

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

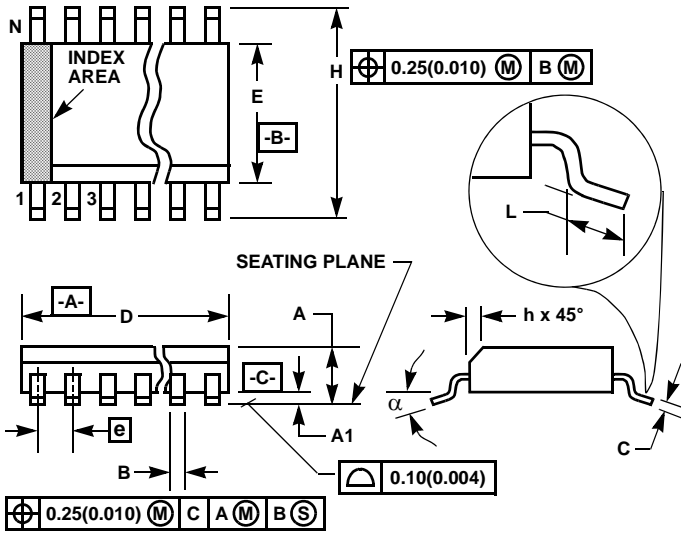
SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

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NOTES:

1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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